AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Withdrawn) A contact line structure for a liquid crystal display device, comprising

a metal line on an array substrate; a silicide layer on the metal line;

an insulating layer having a contact hole exposing a first portion of the silicide layer; and

a transparent conducting terminal in and on the contact hole, wherein the insulating layer is adjacent to the contact hole.

2. (Withdrawn) The contact line structure according to claim 1, wherein the insulating layer includes an organic insulating layer.

3. (Withdrawn) The contact line structure according to claim 2, wherein the organic insulating layer includes one of Benzocyclobutene (BCB) and a photoacrylic resin.

4. (Withdrawn) The contact line structure according to claim 1, wherein the insulating layer includes an inorganic insulating layer and an organic insulating layer.

5. (Withdrawn) The contact line structure according to claim 1, wherein the metal line includes one of a gate pad, a data pad, a drain electrode of a thin film transistor, and a storage upper electrode.

6. (Withdrawn) The contact line structure according to claim 1, wherein the silicide layer is exclusively formed on an upper surface of the metal line.

7. (Withdrawn) The contact line structure according to claim 1, wherein the silicide layer is formed on upper and side surfaces of the metal line.

8. (Withdrawn) The contact line structure of claim 1, wherein the silicide layer is exclusively formed on the first portion of the metal line.

9. (Currently Amended) A method of fabricating a contact line structure for a liquid crystal display device, comprising:

forming a metal line on an array substrate;

forming a silicide layer on the metal line in direct contact with at least a first surface portion of the metal line;

forming an insulating layer having a contact hole exposing a first portion of the silicide layer; and

forming a transparent conducting terminal in and on the contact hole,

wherein the insulating layer is adjacent to the contact hole.

10. (Original) The method according to claim 9, wherein the steps of forming the metal line and the silicide layer include:

depositing a metal material on the array substrate;

forming the silicide layer on the metal material; and

forming the metal line by etching the silicide layer and the metal material.

11. (Original) The method according to claim 9, wherein the steps of forming the metal line and the silicide layer include:

depositing a metal material on the array substrate;

forming the metal line by etching the metal material; and

forming the silicide layer to cover the first portion of the metal line.

12. (Previously Presented) The method according to claim 9, wherein the step of forming the silicide layer is performed before the step of forming an insulating layer.

13. (Original) The method according to claim 9, wherein the metal line includes one of chrome Cr, molybdenum Mo, tungsten W, titanium Ti, tantalum Ta, and a conductive metal alloy.

14. (Original) The method according to claim 9, wherein the step of forming a silicide layer includes a plasma process using a silane group gas containing silicon.

15. (Original) The method according to claim 14, wherein the plasma process is performed at a power of about 100 Watt or less, a pressure of about 110 Pa, a temperature of about 250°C to about 500°C, and a gas flow of about 100 SCCM or less.

16. (Original) The method according to claim 14, wherein the silane group gas is one of SiH_4, Si_2H_6, and Si_3H_8.

17. (Original) The method according to claim 9, wherein the insulating layer includes one of an organic insulating material group containing Benzocyclobutene (BCB) or a photoacrylic resin.

18. (Original) The method according to claim 9, wherein the transparent conducting terminal includes a transparent conducting oxide.

19. (Original) The method according to claim 9, wherein the step of forming a metal line includes simultaneous steps of forming a gate line arranged along a first direction on the array substrate, forming a gate electrode protruding from the gate line, and forming a storage lower electrode in a storage capacitor region of an adjacent gate line.

20. (Original) The method according to claim 19, further comprising:
forming a gate insulating layer on the gate electrode;
forming an active layer on the gate insulating layer above the gate electrode;
forming a data line perpendicular to the gate line to define a pixel region;
simultaneously forming a data pad at one end of the data line, and forming a source electrode above the gate electrode to overlap with a first side of the active layer when forming the data line; and

simultaneously forming a drain electrode to overlap a second side of the active layer at a fixed interval apart from the source electrode, and forming the storage upper electrode in the storage capacitor region of the adjacent gate line when forming the data line.

21. (Original) The method according to claim 9, wherein the transparent conducting terminal is a gate pad terminal.

22. (Original) The method according to claim 21, wherein the step of forming a gate pad terminal includes simultaneously forming a data pad terminal and a pixel electrode.

Claims 23-26 (Canceled).